WHAT IS CLAIMED IS:

1. A data transfer apparatus comprising:

an associative memory connected between a system bus and a local bus; and

a controller for controlling data input/ output of the associative memory;

wherein the controller fetches an address and data that are transferred between devices on the system bus so as to duplicate and store them in the associative memory, accepts a data transfer request from the local bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the associative memory, reads out corresponding data from the associative memory so as to transfer it to the local bus.

2. The data transfer apparatus according to claim 1, wherein, if it is detected that a write cycle of writing a data from one device to another device is generated on the system bus, the controller fetches the address and the data that are transferred between the devices so as to duplicate and store them in the associative memory.

3. The data transfer apparatus according to claim 1, wherein the controller monitors a data output enable signal line of at least one device controller on the system bus and, when the data output enable signal line is asserted, fetches the address and the data that are transferred on the system bus so as to duplicate and store them in the associative memory.

4. The data transfer apparatus according to claim 1, wherein the controller monitors a data output strobe signal line of at least one device controller on the system bus and, when the data output strobe signal line is asserted, fetches the address and the data that are transferred on the system bus so as to duplicate and store them in the associative memory.

5. The data transfer apparatus according to claim 1, wherein, when the address from which the data is transferred indicated by the data transfer request accepted from the local bus is not contained in the address stored in

the associative memory, the controller stores a data effective information indicating the address in which a transfer operation has not been completed in response to the data transfer request in a second associative memory, fetches the address and the data that are transferred between the devices on the system bus and, if the fetched address is the address indicated by the data effective information, transfers it to the local bus as data corresponding to the data transfer request.

6. A data transfer apparatus comprising:

an associative memory connected between a system bus and a local bus; and

a controller for controlling data input/ output of the associative memory;

wherein the controller fetches an address and data that are transferred between devices on the local bus so as to duplicate and store them in the associative memory, accepts a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the associative memory, reads out corresponding data from the associative memory so as to transfer it to the system bus.

7. The data transfer apparatus according to claim 6, wherein, if it is detected that a write cycle of writing a data from one device to another device is generated on the local bus, the controller fetches the address and the data that are transferred between the devices so as to duplicate and store them in the associative memory.

8. The data transfer apparatus according to claim 6, wherein the controller monitors a data output enable signal line of at least one device controller on the local bus and, when the data output enable signal line is asserted, fetches the address and the data that are transferred on the local bus so as to duplicate and store them in the associative memory.

9. The data transfer apparatus according to claim 6, wherein the controller monitors a data output strobe signal line of at least one device controller on the local bus and, when the data output strobe signal line is asserted, fetches the address and the data that are transferred on the local

bus so as to duplicate and store them in the associative memory.

10. The data transfer apparatus according to claim 6, wherein, when the address from which the data is transferred indicated by the data transfer request accepted from the system bus is not contained in the address stored in the associative memory, the controller stores a data effective information indicating the address in which a transfer operation has not been completed in response to the data transfer request in a second associative memory, fetches the address and the data that are transferred between the devices on the local bus and, if the fetched address is the address indicated by the data effective information, transfers it to the system bus as a data corresponding to the data transfer request.

11. A data transfer apparatus comprising:

an associative memory connected between a system bus and a local bus; and

a controller for controlling data input/ output of the associative memory;

wherein the controller fetches an address and data that are transferred between devices on the system bus so as to duplicate and store them in the associative memory, fetches an address and a data that are transferred between devices on the local bus so as to duplicate and store them in the associative memory, accepts a data transfer request from the local bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the associative memory, reads out a corresponding data from the associative memory so as to transfer it to the local bus, accepts a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the associative memory, reads out corresponding data from the associative memory so as to transfer it to the system bus.

12. A data transfer method for controlling data input/ output between a system bus and a local bus, the method comprising:

a buffering operation of fetching an address and data that are transferred between devices on the system bus so as to duplicate and store them; and

an operation of accepting a data transfer request from the local bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the buffering operation, reading out corresponding data so as to transfer it to the local bus.

13. A data transfer method for controlling data input/ output between a system bus and a local bus, the method comprising:

a buffering operation of fetching an address and data that are transferred between devices on the local bus so as to duplicate and store them; and

an operation of accepting a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the buffering operation, reading out corresponding data so as to transfer it to the system bus.

14. A data transfer method for controlling data input/ output between a system bus and a local bus, comprising:

a first buffering operation of fetching an address and data that are transferred between devices on the system bus so as to duplicate and store them;

a second buffering operation of fetching an address and data that are transferred between devices on the local bus so as to duplicate and store them;

a first data transfer operation of accepting a data transfer request from the local bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the first buffering operation, reading out corresponding data so as to transfer it to the local bus; and

a second data transfer operation of accepting a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request is contained in the address stored in the second buffering operation, reading out corresponding data so as to transfer it to the system bus.